REMARKS

Reconsideration of the application is respectfully requested.

The following discussion addresses the issues in the order in which they have been raised in the Office Action.

In this amendment, Applicants have clarified some of the claims without introducing any new matter. In particular, claim 1 has been amended to recite a single chip embodiment of the invention, as well as the claimed *concatenated repair signature*. Although the art references relied upon to date, including U.S. Patent No. 6,577,156 issued to Anand, et al. ("Anand") and U.S. Patent No. 6,249,465 issued to Weiss, et al. ("Weiss") disclose an integrated circuit 10 with a fuse box 11 for repairing memory of the integrated circuit, including decompressing data from the fuse box (Anand), and reducing the number of required fuses so that only an optimum number of defective memory segments can be repaired (Weiss). However, neither reference teaches or suggests the single chip embodiment of Applicants' invention recited in claim 1 that has the capability of composing and applying the *concatenated repair signature* for improved repair performance during in-field testing (as opposed to initial testing before shipping to the customer). Applicants note that another reference cited by the Examiner, the article by Michael R. Ouellette "Shared Fuse Macro for Multiple Embedded Memory Devices with Redundancy", does describe an ASIC design with embedded memory which have redundant elements, and a defect repair methodology in which fuse data has been compressed. See Fig. 2 of that article which shows an example fuse value shift register data string. This reference, however, does not teach or suggest the arrangement of bit strings as recited in Applicants' claimed *concatenated repair signature*. See Applicants' Specification, Fig. 4 for an example of such repair signature.

The amendments made to dependent claims 2-4, 6, 8, 9 and 15 are merely to clarify the language and do not narrow their scope.

Turning now to independent claim 16, this claim recites an apparatus having a memory test and repair capability of a *concatenated repair signature* as explained above in connection with claim 1, except there may be one or more bits in each field that identifies the respective memory. None of the relied upon art references teach or

suggest such a repair signature that can be advantageously used on every cycle that the device is initialized.

Referring now to claim 22, this claim has also been amended in a manner similar to claim 16 and also recites that the fuse box *contains an amount of non-volatile fuses to provide actual repair capability for only a subset, that is not all, of the memories that share the fuse box*. The relied upon art references do not teach or suggest such an apparatus.

As to claim 27, this claim has now been amended to recite a method that composes a concatenated repair signature which is not taught or suggested by the prior art.

Claims 30, 35, and 37 also recite the novel concatenated repair signature.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language, including the right to swear behind or otherwise remove an improper art reference.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No.

02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: June 20, 2007.

By _____
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CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on June 20, 2007.

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Margaux Rodriguez *June 20, 2007*